11.(Amended) A method of manufacturing a trench isolation layer, the method comprising:

(a) sequentially forming a pad oxide layer and a hard mask layer on a semiconductor substrate;

(b) patterning the hard mask layer and the pad oxide layer by photolithography to form a hard mask pattern and a pad oxide pattern;

(c) etching a portion of the semiconductor substrate using the hard mask pattern as a mask to thereby form a shallow trench;

(d) forming a thermal oxide layer along inner walls of the semiconductor substrate that define opposed side walls and a bottom wall of the shallow trench, such that the thermal oxide layer has a central portion disposed along the inner wall of the substrate that defines the bottom of the shallow trench, and lateral portions disposed along the inner walls of the substrate that define the opposed side walls of the shallow trench, respectively, the lateral portions each having a curvilinear sectional profile at an interface with the upper surface of the semiconductor substrate;

(e) etching the resulting structure using the hard mask pattern as a mask to extend said shallow trench deeper into the semiconductor substrate and thereby form a deep trench, wherein the central portion of the thermal oxide layer is removed, and the lateral portions of the thermal oxide are left in place;

(f) forming a buffer layer over the entire upper surface of the structure in which the deep trench has been formed;

(g) filling the deep trench, in which the buffer layer has been formed, with a first oxide layer;

(h) planarizing the resulting structure in which the deep trench has been filled with the first oxide layer; and

(i) removing the hard mask pattern.

12.(Amended) The method of claim 11, and further comprising the step of forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern, and wherein step (c) comprises etching a portion of the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the shallow trench, and step (e) comprises etching the central portion of the thermal oxide layer and the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the deep trench.

14.(Amended) The method of claim 13, and further comprising the step of forming a second oxide layer between the liner and the first oxide layer.

17.(Amended) A method of manufacturing a trench isolation layer, the method comprising:

(a) sequentially forming a pad oxide layer and a hard mask layer on a flat upper surface of a semiconductor substrate;

(b) patterning the hard mask layer and the pad oxide layer using photolithography to form a hard mask pattern and a pad oxide pattern on the flat upper surface of the semiconductor substrate;

(c) forming a thermal oxide layer on a portion of the flat upper surface of the semiconductor substrate between respective portions of the pad oxide pattern, such that the thermal oxide layer has a central portion, and lateral portions each having the sectional profile of a bird's beak at an interface with the upper surface of the semiconductor substrate;

(d) etching the resulting structure using the hard mask pattern as a mask to thereby form a deep trench, wherein the central portion of the thermal oxide layer is removed, and the lateral portions of the thermal oxide are left at the interface with the upper surface of the semiconductor substrate;

(e) forming a buffer layer over the entire upper surface of the resulting structure in which the deep trench has been formed;

(f) filling the deep trench, in which the buffer layer has been formed, with a first oxide layer;

(g) planarizing the resulting structure in which the deep trench has been filled with the first oxide layer; and

(h) removing the hard mask pattern.

18.(Amended) The method of claim 17, and further comprising the step of forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern, and wherein step (d) comprises etching the central portion of the thermal oxide layer and the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the deep trench.

Please add the following new claims 22-28:

22. (New) The method of claim 12, wherein the step of forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern is performed before the shallow trench is formed in step (c).

23. (New) The method of claim 11, wherein step (e) comprises removing the entire portion of the thermal oxide layer that is disposed along the bottom of the shallow trench, such that the etching forms a deep trench that has substantially the same width as the shallow trench.

24. (New) The method of claim 12, wherein step (e) comprises etching the resultant structure using only the hard mask and the spacer as a mask, thereby removing the entire portion of the thermal oxide layer that is disposed along the bottom of the shallow trench, whereby the etching forms a deep trench that has substantially the same width as the shallow trench.

25.(New) The method of claim 11, wherein step (f) comprises forming one of a high temperature oxide layer, a middle temperature oxide layer and a plasma-enhanced oxide layer as the buffer layer.

26. (New) The method of claim 17, wherein step (d) comprises removing the entire portion of the thermal oxide layer that extends between the lateral portions having the sectional profile of a bird's beak.

27. (New) The method of claim 12, wherein step (d) comprises etching the resultant structure using only the hard mask and the spacer as a mask, thereby removing the entire portion of the thermal oxide layer that extends between the lateral portions having the sectional profile of a bird's beak.

28.(New) The method of claim 17, wherein step (e) comprises forming one of a high temperature oxide layer, a middle temperature oxide layer and a plasma-enhanced oxide layer as the buffer layer.

REMARKS

The Office Action of September 25, 2002 and the references cited therein have been carefully studied and reviewed, and in view of the foregoing Amendment and following representations, reconsideration is respectfully requested.

At the outset, Applicants do not understand why the Examiner has found the Title of the invention to not be descriptive. Applicants have reviewed the Titles of the very patents cited by the Examiner in the Office Action, such as USP 5,910,018 to Jang, entitled "Trench Edge Rounding Method and Structure For Trench Isolation". The Title of the present application is at least, if not more, descriptive than the titles of the prior art patents. It is thus respectfully requested that the Examiner withdraw the requirement for a new Title.

Next, the preamble of claim 11 has been changed so as to correspond to that of claim 17. Accordingly, the Examiner's objection to claim 11 has been rendered moot.